AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A circuit arrangement ~~for protecting integrated semiconductor circuits from electrical pulses or electrical overvoltages, said circuit arrangement having~~ comprising:

[[-]] ~~an RC~~ a resistive-capacitive (RC) element ~~which comprises a first resistor (R1; R10) and a capacitance (C1; C10) and is~~ connected between ~~two~~ a first supply potential line and a second supply potential line, the RC element including:

a first resistor; and ~~lines (VDD, VSS),~~

a first capacitor;

[[-]] a plurality ~~chain~~ of inverters ~~(I10 - I12) which are~~ connected in series and having junction points between inverters in the plurality of inverters, an ~~the~~ input of said ~~chain~~ plurality of inverters being connected to ~~the junction~~ a point between the first resistor ~~(R1; R10)~~ and the ~~capacitance (C1; C10)~~ first capacitor, [[and]]

[[-]] ~~having~~ a protection transistor having a control input, a first input, and a first output, wherein the ~~(ST) whose~~ control input is connected to the output of the plurality of inverters at a junction point, ~~inverter chain and whose outputs are connected~~ the first inut is connected to the

first supply potential line, and the first output is connected to the second ~~to the two~~ supply potential ~~lines (VDD, VSS)~~ line, and ~~characterized in that~~

a plurality of resistors, a first input of each of the resistors being connected to a different one of the junction points between the plurality of inverters ~~(I10—I12)~~ and the junction point between the inverters and the protection transistor, ~~(ST) are each connected to a resistor (R11, R12, R13), with the~~ and a second input of each of the resistors being connected to ~~respective other connection of the resistors being connected to~~ one of the first supply potential ~~lines (VDD, VSS)~~ line and the second supply potential line.

2. (Currently Amended) The circuit arrangement of ~~as claimed in~~ claim 1, ~~characterized in that~~ wherein the resistors are alternately connected to the first supply ~~each of the supply~~ potential ~~lines (VDD, VSS)~~ line and the second supply potential line.

3. (Currently Amended) The circuit arrangement ~~as claimed in claim 1 or 2~~ of claim 1, ~~characterized in that~~ wherein an [[the]] input of [[the]] a last inverter ~~(I12)~~ in the plurality of inverters ~~inverter chain~~ is connected to one of the first supply potential line and the second supply potential line ~~(VDD) via~~ by a first resistor of the plurality of ~~one of the~~ resistors ~~(R11)~~, and an [[the]] output of the last inverter ~~(I12) inverter chain~~ is connected to the other of the first supply potential line and the second supply potential line ~~(VSS) via another one~~ by a second resistor of the plurality of resistors ~~(R12)~~ and the output of the last inverter is connected to the control input of the protection transistor ~~(ST)~~.

4. (Currently Amended) The circuit arrangement ~~as claimed in one of claims 1 to 3~~ of claim 1, ~~characterized in that~~ wherein the inverters comprise ~~are in the form of~~ CMOS inverters. ~~(P10, N10; P11, N11; P12, N12).~~

5. (Currently Amended) The circuit arrangement ~~as claimed in one of claims 1 to 4~~ of claim 1, ~~characterized in that~~ wherein the resistors comprise ~~are in the form of~~ diffusion resistances.

6. (Currently Amended) The circuit arrangement ~~as claimed in one of claims 1 to 5~~ of claim 1, ~~characterized in that~~ wherein the first resistor comprises ~~(R10) is~~ a diffusion resistance.

7. (Currently Amended) The circuit arrangement ~~as claimed in one of claims 1 to 6~~ of claim 1, ~~characterized in that~~ wherein the capacitance comprises ~~(C1; C10) is~~ an oxide capacitance.

8. (New) The circuit arrangement of claim 1, wherein the circuit arrangement is configured to protect integrated semiconductor circuits from electrical pulses or electrical overvoltages.

9. (New) A circuit arrangement comprising:

an resistive-capacitive (RC) element connected between a first supply potential line and a second supply potential line, the RC element including:

a first resistor; and

a first capacitor;

a first inverter having an input and an output, wherein the input of the first inverter is connected to a first node between the first resistor and the first capacitor;

a second inverter having an input and an output, wherein the input of the second inverter is connected to the output of the first inverter at a second node;

a third inverter having an input and an output, wherein the input of the third inverter is connected to the output of the second inverter at a third node;

a protection transistor having a control input, a first input, and a first output, wherein the control input is connected to the output of the third inverter at a fourth node, wherein the first input of the protection transistor is connected to a first supply potential line, and the first output of the protection transistor is connected to a second supply potential line, and

a first resistor connected between the second node and the first supply potential line,

a second resistor connected between the third node and the second supply potential line, and

a third resistor connected between the fourth node and the first supply potential line.

10. (New) The circuit arrangement of claim 9, wherein the first, second, and third inverters comprise CMOS inverters.

11. (New) The circuit arrangement of claim 9, wherein the resistors are diffusion resistances.

12. (New) The circuit arrangement of claim 9, wherein the first resistor comprises a diffusion resistance.

13. (New) The circuit arrangement of claim 9, wherein the capacitance comprises an oxide capacitance.